AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) A method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus;

(b) receiving a first address-byte on the bus;

(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte;

(d) selecting a first one of the at least two registers, the first register corresponding with the first count; and

(e) storing the first address-byte in the selected first register.

2. (previously presented) The method of claim 1, further comprising:

receiving a second address-byte;

producing a second count of address bytes received on the bus as a result of receiving the second address-byte;

selecting a second one of the at least two registers, the second register corresponding with the second count; and

storing the second address-byte in the selected second register.

3. (previously presented) The method of claim 2, further comprising the steps of:

receiving a memory access command; and

accessing the memory space at an_address defined by the first and second address-bytes as a result of the memory access command.

4. (previously presented) The method of claim 3, wherein the memory access command is a write command.

5. (previously presented) The method of claim 3, wherein the memory access command is a read command.

6. (previously presented) The method of claim 3, wherein the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte.

7. (previously presented) The method of claim 6, wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte.

8. (cancelled)

9. (cancelled)

10. (previously presented) The method of claim 1, further comprising a step of providing a memory, wherein the 2^M address memory space comprises the address space of the memory.

11. (previously presented) The method of claim 1, further comprising a step of providing at least two memories, wherein the 2^M address memory space comprises the address space of the at least two memories.

12. (currently amended) An apparatus for high speed addressing of a memory space having 2^M addresses, comprising:

(a) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus;

(b) an N-bit bus, where M is greater than N;

(c) first and second control signal lines; and

(d)~~(c)~~a logic circuit coupled with the bus, the first and second control signal lines, and the at least two registers, the logic circuit to select one of the at least two registers, the logic circuit including:

(i) a K-bit ~~an~~ address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal

line, wherein the number of the at least two registers is less than or equal to 2^K; and

(ii) a selecting unit to select one of the at least two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter.

13. (previously presented) The apparatus of claim 12, wherein the logic circuit stores a received address-byte in a selected one of the at least two registers.

14. (previously presented) The apparatus of claim 13, further comprising a unit to:

receive a memory access command; and

access the memory space at an address defined by the first and second address-bytes as a result of the memory access command.

15. (previously presented) The apparatus of claim 14, wherein the memory access command is a write command.

16. (previously presented) The apparatus of claim 14, wherein the memory access command is a read command.

17. (previously presented) The apparatus of claim 14, wherein the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte.

18. (previously presented) The apparatus of claim 17, wherein the unit receives the memory access command in a next subsequent bus transaction following receipt of the second address-byte.

19. (cancelled)

20 (cancelled)

21. (previously presented) The apparatus of claim 12, further comprising a memory, the addresses of which are defined by the 2^M address memory space.

22. (previously presented) The apparatus of claim 12, further comprising at least two memories, the addresses of which are defined by the 2^M address memory space.

23. (currently amended) A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus, where M is greater than N, comprising the steps of:

(a) receiving a first address-byte on the bus;

(b) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte;

(c) selecting a first one of the at least two registers, the first register corresponding with the first count; and

(d) storing the first address-byte ~~byte~~ in the selected first register.

24. (previously presented) The machine readable medium of claim 23, the method further comprising the steps of:

receiving a second address-byte;

producing a second count of address-bytes received on the bus as a result of receiving the second address-byte;

selecting a second one of the at least two registers, the second register corresponding with the second count; and

storing the second address-byte in the selected second register.

25. (previously presented) The machine readable medium of claim 24, the method further comprising the steps of:

receiving a memory access command; and

accessing a memory at an address defined by the first and second address-bytes as a result of the memory access command.

26. (previously presented) The machine readable medium of claim 25, wherein the memory access is a write access.

27. (previously presented) The machine readable medium of claim 25, wherein the memory access is a read access.

28. (previously presented) The machine readable medium of claim 25, wherein the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte.

29. (previously presented) The method of claim 28, wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte.

30. (cancelled)

31. (cancelled)

32. (previously presented) The machine readable medium of claim 23, wherein the 2^M address memory space comprises the address space of a memory.

33. (previously presented) The machine readable medium of claim 23, wherein the 2^M address memory space comprises the address space of at least two memories.

34. (cancelled)

35. (cancelled)

36. (cancelled)

37. (currently amended) A ~~An~~ system, comprising:

(a) an N-bit bus, where M is greater than N;

(b) a memory having 2^M addresses;

(c) a central processing unit, coupled with the bus, to transmit at least two address-bytes that together define an address in the memory space and to transmit a memory access command;~~.~~

(d) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory, each register associated with a particular count of address-bytes received on the bus; ~~and~~

(e) first and second control signal lines;

(f)(e) a logic circuit coupled with the bus, the first and second control signal lines, and the at least two registers, the logic circuit to receive and store address-bytes in a selected one of the at least two registers, the logic circuit including:

(i) a K-bit ~~an~~ address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal line, wherein the number of the at least two registers is less than or equal to 2^K; and

(ii) a selecting unit to select one of the at least two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter; and

(g)(f) a unit to:

(i) receive the memory access command; and

(ii) access the memory at an address defined by the first and second address-bytes as a result of the memory access command.

38. (previously presented) The system of claim 37, wherein the memory access command is a write command.

39. (previously presented) The system of claim 37, wherein the memory access command is a read command.

40. (previously presented) The system of claim 37, wherein the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte.

41. (previously presented) The system of claim 40, wherein the unit receives the memory access command in a next subsequent bus transaction following receipt of the second address-byte.

42. (cancelled)

43. (new) The method of claim 3, wherein the write command transfers data on the N-bit bus.

44. (new) The method of claim 4, wherein the read command transfers data on the N-bit bus.

45. (new) The apparatus of claim 12, wherein K equals one.

46. (new) The apparatus of claim 12, wherein K equals two.

47. (new) The of machine readable medium claim 26, wherein the write access transfers data on the N-bit bus.

48. (new) The machine readable medium of claim 27, wherein the read access transfers data on the N-bit bus.

49. (new) The system of claim 37, wherein K equals one.

50. (new) The system of claim 37, wherein K equals two.